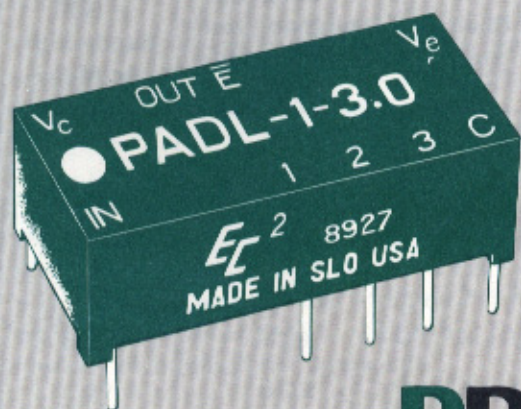


EC²



low profile

DIP

3-BIT

PROGRAMMABLE ANALOG DELAY LINE

- Analog input and output
- All delays digitally programmable
- Delays stable and precise
- 14-pin DIP package (.240 high)
- Available in delays up to 36ns
- Available in 10 delay steps with resolution from .5 to 5ns

design notes

The "DIP Series" of Programmable Analog Delay Lines developed by Engineered Components Company have been designed to allow for final delay adjustment during or after installation in a circuit. These Programmable Analog Delay Lines incorporate required control circuitry to pick-off analog signals, and are contained in a 14-pin DIP package. These

modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 1.6 million hours. The design includes internal termination; no additional external components are needed to obtain the required delay.

These Programmable Analog Delay Lines are digitally programmable by the presence of either a T²L "1" or a "0" at each of the programming pins. Since the input and the output terminals are fixed and the programming is accomplished only by DC voltage levels, programming may be accomplished by remote switching or permanent termination of the appropriate programming pins; the Delay Line may also be programmed automatically by computer generated data. MUX set-up time is 24ns typical.

The PADL is offered in 10 models with time delays to a maximum of 36ns and with step resolution as shown in the Part Number Table. Programming of maximum delays is accomplished in 8 delay steps in accordance with the Truth Table examples

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