

EC²



low profile
SIP
LUMPED
CONSTANT
PASSIVE DELAY LINE

- Analog input and outputs
- Delays stable and precise
- 7-pin SIP package (.230 high)
- Available in delays from 5 to 200ns
- Five (5) equally-spaced taps
- Available in impedances of 50, 100 and 200 ohms

design notes

The "SIP Series" Lumped Constant Passive Delay Lines developed by Engineered Components Company have been designed to provide precise delays for analog delay line applications. These delay lines provide excellent delay accuracy, low DCR, low attenuation and low distortion.

These delay lines are offered in 38 models with delays from 5 to 200ns and with taps at 20% increments of total delay. Delay time is measured at the 50% point on the leading edge. Accuracies are maintained as shown under "Operating Characteristics." Temperature coefficient of delay is less than 75 ppm/°C over the operating temperature range of -55 to +125°C.

"SIP Series" LC delay lines are intended for use in most analog applications; they are also compatible with the low signal levels of TTL and ECL. These delay lines find extensive use in

providing the required delay timing functions necessary in radar, computer, communication, testing and instrument applications.

Construction of the "SIP Series" utilizes miniature inductors and monolithic ceramic capacitors to provide the utmost in miniaturization and reliability. The MTBF on these delay lines, when calculated per MIL-HDBK-217, for a 50°C ground fixed environment and with 5V DC applied, is in excess of 12 million hours.

The "SIP Series" delay lines are packaged in a 7-pin SIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F. These delay lines are designed to meet the applicable portions of MIL-D-23859, and they are capable of meeting the environmental requirements of MIL-STD-202 for moisture resistance, vibration, temperature cycling, humidity and life. Flat metal leads meet the solderability requirements of MIL-STD-202, Method 208. Corner standoffs on the housing provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

Marking consists of manufacturer's name, part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

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