

PART NUMBER TABLE

*Suffix Part Number with G (for Gull Wing Lead), J (for J Lead), F (for Thru-hole Lead) or T (for Tucked Lead). Examples: PFLDL-TTL-5-50G (Gull Wing), PFLDL-TTL-5-7J (J Lead), PFLDL-TTL-5-8F (Thru-hole Lead) or PFLDL-TTL-5-15T (Tucked Lead).

∅ DELAYS AND TOLERANCES (in ns)				
PART NUMBER	*STEP ZERO DELAY TIME	MAXIMUM DELAY TIME (NOM)	DELAY CHANGE PER STEP	**MAXIMUM DEVIATION FROM PROGRAMMED DELAY
PFLDL-TTL-5-5	5.0 ± 1	8.5	.5 ± .3	± .4
PFLDL-TTL-5-1	5.0 ± 1	12	1 ± .3	± .4
PFLDL-TTL-5-2	5.0 ± 1	19	2 ± .4	± .6
PFLDL-TTL-5-3	5.0 ± 1	26	3 ± .5	± .8
PFLDL-TTL-5-4	5.0 ± 1	33	4 ± .5	± .9
PFLDL-TTL-5-5	5.0 ± 1	40	5 ± .5	± 1.0
PFLDL-TTL-5-6	5.0 ± 1	47	6 ± .6	± 1.2
PFLDL-TTL-5-7	5.0 ± 1	54	7 ± .7	± 1.4
PFLDL-TTL-5-8	5.0 ± 1	61	8 ± .8	± 1.6
PFLDL-TTL-5-9	5.0 ± 1	68	9 ± .9	± 1.8
PFLDL-TTL-5-10	5.0 ± 1	75	10 ± 1.0	± 2.0
PFLDL-TTL-5-11	5.0 ± 1	82	11 ± 1.1	± 2.2
PFLDL-TTL-5-12	5.0 ± 1	89	12 ± 1.2	± 2.4
PFLDL-TTL-5-13	5.0 ± 1	96	13 ± 1.3	± 2.6
PFLDL-TTL-5-14	5.0 ± 1	103	14 ± 1.4	± 2.8
PFLDL-TTL-5-15	5.0 ± 1	110	15 ± 1.5	± 3.0
PFLDL-TTL-5-20	5.0 ± 1	145	20 ± 2.0	± 4.0
PFLDL-TTL-5-25	5.0 ± 1	180	25 ± 2.5	± 5.0
PFLDL-TTL-5-30	5.0 ± 1	215	30 ± 3.0	± 6.0
PFLDL-TTL-5-35	5.0 ± 1	250	35 ± 3.5	± 7.0
PFLDL-TTL-5-40	5.0 ± 1	285	40 ± 4.0	± 8.0
PFLDL-TTL-5-45	5.0 ± 1	320	45 ± 4.5	± 9.0
PFLDL-TTL-5-50	5.0 ± 1	355	50 ± 5.0	± 10.0

TRUTH TABLE EXAMPLES

PROGRAMMING PINS PART NUMBER	3	0	0	0	0	1	1	1	1
	2	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0	1
PFLDL-TTL-5-1		5	1	2	3	4	5	6	7
PFLDL-TTL-5-2		5	2	4	6	8	10	12	14
PFLDL-TTL-5-3		5	3	6	9	12	15	18	21
ETC.									

* Delay at step zero is referenced to the input pin.

** All delay times after step zero are referenced to step zero.

∅ All modules can be operated with a minimum input pulse width of 40% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.