

## PART NUMBER TABLE

φ DELAYS AND TOLERANCES (in ns)				
Part Number	*Step Zero Delay Time	Maximum Delay Time (Nom)	Delay Change Per Step	** Maximum Deviation From Programmed Delay
PECLDL-2.8-0.1	2.8±.2	4.3	0.1±.04	±.1
PECLDL-2.8-0.2	2.8±.2	5.8	0.2±.05	±.2
PECLDL-2.8-0.3	2.8±.2	7.3	0.3±.1	±.25
PECLDL-2.8-0.4	2.8±.2	8.8	0.4±.1	±.3
PECLDL-2.8-0.5	2.8±.2	10.3	0.5±.15	±.35
PECLDL-2.8-0.6	2.8±.2	11.8	0.6±.15	±.4
PECLDL-2.8-0.7	2.8±.2	13.3	0.7±.2	±.45
PECLDL-2.8-0.8	2.8±.2	14.8	0.8±.2	±.5
PECLDL-2.8-0.9	2.8±.2	16.3	0.9±.2	±.5
PECLDL-2.8-1.0	2.8±.2	17.8	1.0±.2	±.5
PECLDL-2.8-1.5	2.8±.2	25.3	1.5±.25	±.8
PECLDL-2.8-2.0	2.8±.2	32.8	2.0±.25	±1.0
PECLDL-2.8-2.5	2.8±.2	40.3	2.5±.3	±1.3
PECLDL-2.8-3.0	2.8±.2	47.8	3.0±.3	±1.5
PECLDL-2.8-3.5	2.8±.2	55.3	3.5±.35	±1.8
PECLDL-2.8-4.0	2.8±.2	62.8	4.0±.4	±2.0
PECLDL-2.8-4.5	2.8±.2	70.3	4.5±.45	±2.3
PECLDL-2.8-5.0	2.8±.2	77.8	5.0±.5	±2.5

## TRUTH TABLE EXAMPLES

Part Number \ Programming Pins	4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
PECLDL-2.8-0.1	2.8	.1	.2	.3	.4	.5	.6	.7	.8	.9	1.0	1.1	1.2	1.3	1.4	1.5	
PECLDL-2.8-0.5	2.8	.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5	
PECLDL-2.8-2.0	2.8	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	
ETC.																	

\* Delay at step zero is referenced to the input pin.

\*\*All delay times after step zero are referenced to step zero.

φ All modules can be operated with a minimum input pulse width of 2ns or 20% of full delay, whichever is greater, and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. [Special modules can be readily manufactured to improve accuracies and/or provide customer specified delay times for specific applications.](#)