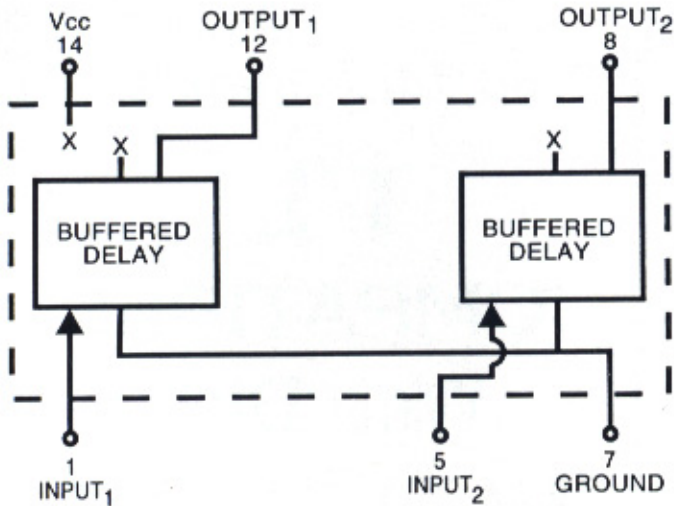


**BLOCK DIAGRAM IS SHOWN BELOW**

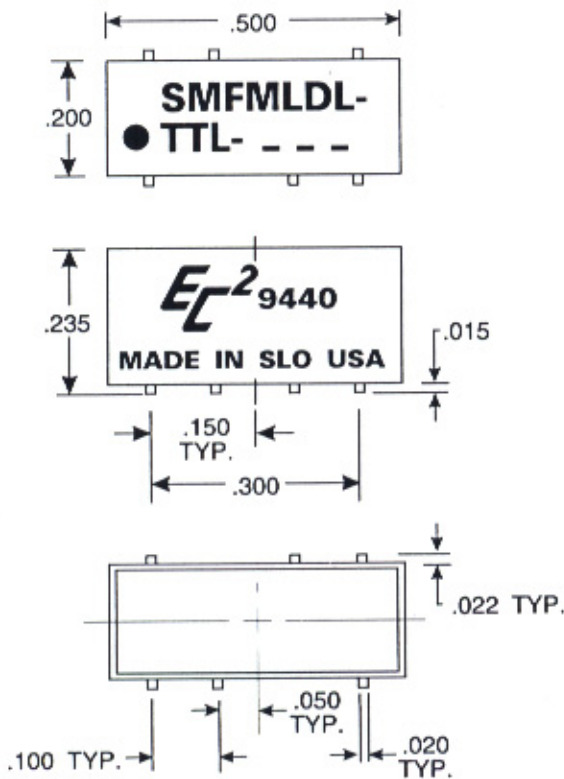


**OPERATING SPECIFICATIONS**

- \*  $V_{cc}$  supply voltage: . . . . . 4.75 to 5.25V DC
- $V_{cc}$  supply current:
  - Constant "0" in . . . . . 60mA typical
  - Constant "1" in . . . . . 7mA typical
- Logic 1 Input:
  - Voltage . . . . . 2V min.;  $V_{cc}$  max.
  - Current . . . . . 2.7V = 20uA max.
  - 5.5V = 1mA max.
- Logic 0 Input:
  - Voltage . . . . . .8V max.
  - Current . . . . . -6mA max.
- Logic 1 Voltage out: . . . . . 2.7V min.
- Logic 0 Voltage out: . . . . . .5V max.
- Operating temperature range: . . . . . 0 to 70°C.
- Storage temperature: . . . . . -55 to +125°C.

\* Delays increase or decrease approximately 2% for a respective increase or decrease of 5% in supply voltage.

**MECHANICAL DETAIL IS SHOWN BELOW**



**PART NUMBER TABLE**

∅ DELAYS AND TOLERANCES (in ns)			
PART NO.	OUTPUT	PART NO.	OUTPUT
SMFMLDL-TTL-5	5 ± 1	SMFMLDL-TTL-30	30 ± 1.5
SMFMLDL-TTL-6	6 ± 1	SMFMLDL-TTL-35	35 ± 1.5
SMFMLDL-TTL-7	7 ± 1	SMFMLDL-TTL-40	40 ± 1.5
SMFMLDL-TTL-8	8 ± 1	SMFMLDL-TTL-45	45 ± 2
SMFMLDL-TTL-9	9 ± 1	SMFMLDL-TTL-50	50 ± 2
SMFMLDL-TTL-10	10 ± 1	SMFMLDL-TTL-55	55 ± 2
SMFMLDL-TTL-11	11 ± 1	SMFMLDL-TTL-60	60 ± 2
SMFMLDL-TTL-12	12 ± 1	SMFMLDL-TTL-65	65 ± 2.5
SMFMLDL-TTL-13	13 ± 1	SMFMLDL-TTL-70	70 ± 2.5
SMFMLDL-TTL-14	14 ± 1	SMFMLDL-TTL-75	75 ± 2.5
SMFMLDL-TTL-15	15 ± 1	SMFMLDL-TTL-80	80 ± 2.5
SMFMLDL-TTL-16	16 ± 1	SMFMLDL-TTL-85	85 ± 3
SMFMLDL-TTL-17	17 ± 1	SMFMLDL-TTL-90	90 ± 3
SMFMLDL-TTL-18	18 ± 1	SMFMLDL-TTL-95	95 ± 3
SMFMLDL-TTL-19	19 ± 1	SMFMLDL-TTL-100	100 ± 3
SMFMLDL-TTL-20	20 ± 1	SMFMLDL-TTL-125	125 ± 4
SMFMLDL-TTL-21	21 ± 1	SMFMLDL-TTL-150	150 ± 4.5
SMFMLDL-TTL-22	22 ± 1	SMFMLDL-TTL-175	175 ± 5
SMFMLDL-TTL-23	23 ± 1	SMFMLDL-TTL-200	200 ± 6
SMFMLDL-TTL-24	24 ± 1	SMFMLDL-TTL-225	225 ± 7
SMFMLDL-TTL-25	25 ± 1	SMFMLDL-TTL-250	250 ± 8

**TEST CONDITIONS**

1. All measurements are made at 25°C.
2.  $V_{cc}$  supply voltage is maintained at 5.0V DC.
3. All units are tested using a FAST toggle-type positive input pulse and one FAST T<sup>2</sup>L load at the output being tested.
- ∅ 4. Input pulse width used is 5 to 10ns longer than full delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

∅ All modules can be operated with a minimum input pulse width of 100% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. **Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.**