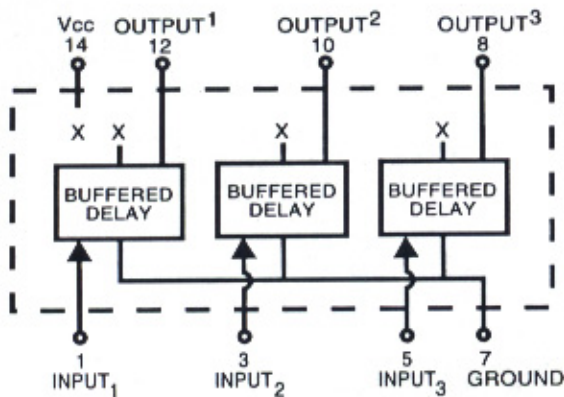
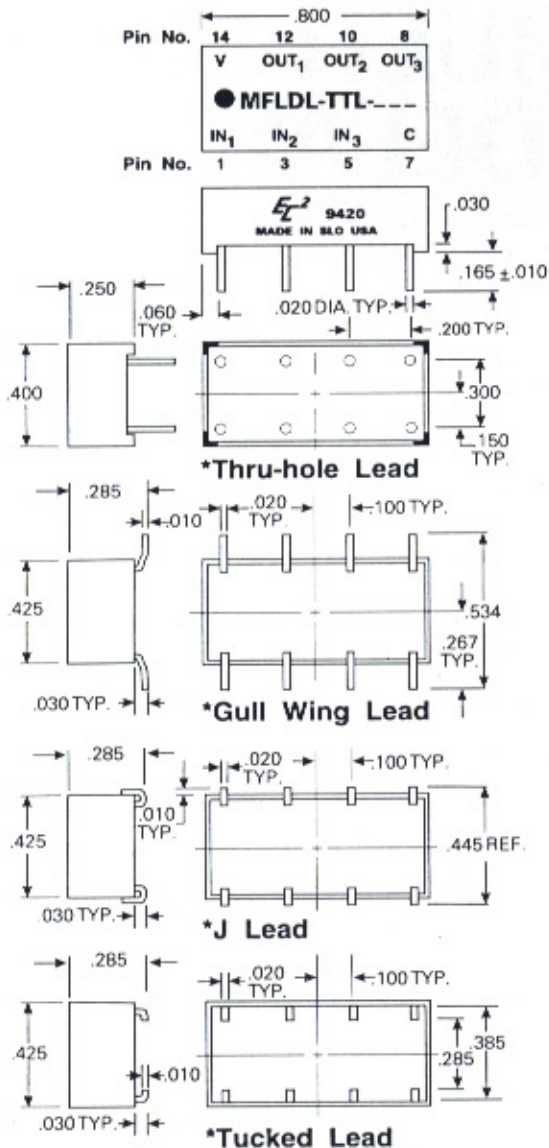


## BLOCK DIAGRAM IS SHOWN BELOW



## MECHANICAL DETAIL IS SHOWN BELOW



## OPERATING SPECIFICATIONS

$V_{CC}$ supply voltage:	4.75 to 5.25V DC
$V_{CC}$ supply current:	
Constant "0" in	85mA typical
Constant "1" in	5mA typical
Logic 1 Input:	
Voltage	2V min.; $V_{CC}$ max.
Current	2.7V = 20 $\mu$ A max. 5.5V = 1mA max.
Logic 0 Input:	
Voltage	.8V max.
Current	-.6mA max.
Logic 1 Voltage out:	2.7V min.
Logic 0 Voltage out:	.5V max.
Operating temperature range:	0 to +70°C
Storage temperature:	-55 to +125°C.

Delays increase or decrease approximately 4% for a respective increase or decrease of 5% in supply voltage.

## PART NUMBER TABLE

\* Suffix Part Number with G (for Gull Wing Lead), J (for J Lead), F (for Thru-hole Lead) or T (for Tucked Lead).  
Examples: MFLDL-TTL-10G (Gull Wing), MFLDL-TTL-25J (J Lead), MFLDL-TTL-75F (Thru-hole Lead) or MFLDL-TTL-80T (Tucked Lead).

Ø DELAYS AND TOLERANCES (in ns)			
PART NO.	OUTPUT	PART NO.	OUTPUT
MFLDL-TTL-5	5 ± 1	MFLDL-TTL-30	30 ± 1.5
MFLDL-TTL-6	6 ± 1	MFLDL-TTL-35	35 ± 1.5
MFLDL-TTL-7	7 ± 1	MFLDL-TTL-40	40 ± 1.5
MFLDL-TTL-8	8 ± 1	MFLDL-TTL-45	45 ± 2
MFLDL-TTL-9	9 ± 1	MFLDL-TTL-50	50 ± 2
MFLDL-TTL-10	10 ± 1	MFLDL-TTL-55	55 ± 2
MFLDL-TTL-11	11 ± 1	MFLDL-TTL-60	60 ± 2
MFLDL-TTL-12	12 ± 1	MFLDL-TTL-65	65 ± 2.5
MFLDL-TTL-13	13 ± 1	MFLDL-TTL-70	70 ± 2.5
MFLDL-TTL-14	14 ± 1	MFLDL-TTL-75	75 ± 2.5
MFLDL-TTL-15	15 ± 1	MFLDL-TTL-80	80 ± 2.5
MFLDL-TTL-16	16 ± 1	MFLDL-TTL-85	85 ± 3
MFLDL-TTL-17	17 ± 1	MFLDL-TTL-90	90 ± 3
MFLDL-TTL-18	18 ± 1	MFLDL-TTL-95	95 ± 3
MFLDL-TTL-19	19 ± 1	MFLDL-TTL-100	100 ± 3
MFLDL-TTL-20	20 ± 1	MFLDL-TTL-125	125 ± 4
MFLDL-TTL-21	21 ± 1	MFLDL-TTL-150	150 ± 4.5
MFLDL-TTL-22	22 ± 1	MFLDL-TTL-175	175 ± 5
MFLDL-TTL-23	23 ± 1	MFLDL-TTL-200	200 ± 6
MFLDL-TTL-24	24 ± 1	MFLDL-TTL-225	225 ± 7
MFLDL-TTL-25	25 ± 1	MFLDL-TTL-250	250 ± 8

## TEST CONDITIONS

- All measurements are made at 25°C.
- $V_{CC}$  supply voltage is maintained at 5.0V DC.
- All units are tested using a FAST toggle-type positive input pulse and one FAST T<sup>2</sup>L load at the output.
- Input pulse width used is 100% longer than delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

Ø All modules can be operated with a minimum input pulse width of 100% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. **Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.**