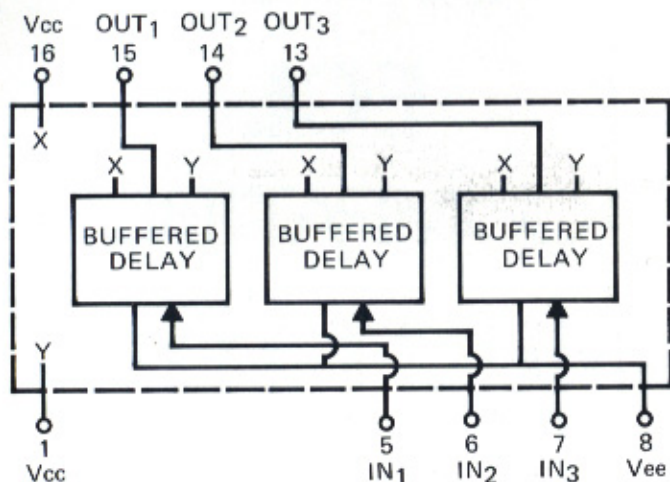


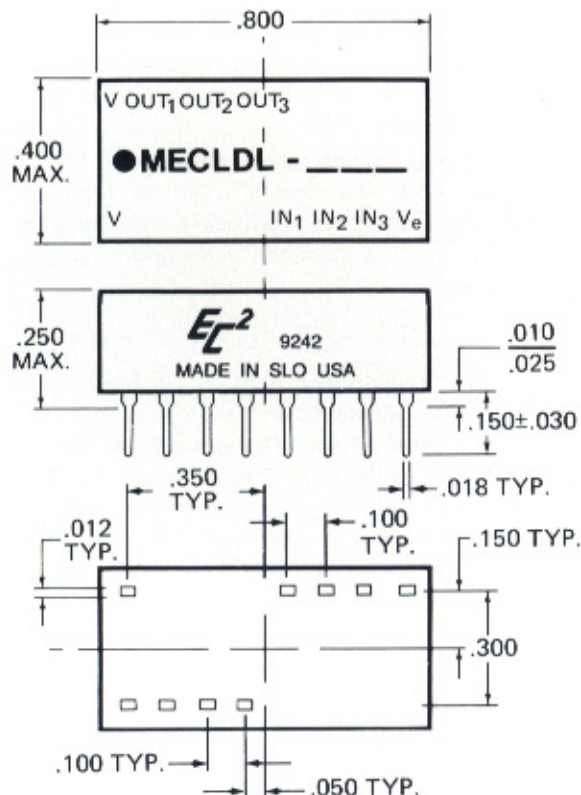
DESIGN NOTES (continued)

Marking consists of manufacturer's name, logo (EC²), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITIONS

- All measurements are made at 25°C.
- Vee supply voltage is maintained at -5.2V DC.
- All units are tested using a positive input pulse provided by a standard open emitter ECL 10,000 gate. The input and output utilize a 100 ohm pulldown resistor to -2V; the output is also loaded with one ECL 10,000 gate.
- Input pulse width used is 100% longer than delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

OPERATING SPECIFICATIONS

- Supply voltage: -5.2V ±5% to Vee (can be operated on +5V to Vcc).
- Supply current: 90ma typical
- Logic 1 input at 25°C:
 - Voltage -.98 min.
 - Current 265ua max.
- Logic 0 input at 25°C:
 - Voltage -1.63 max.
 - Current5ua min.
- Logic 1 Voltage out at 25°C: -.96 min.
- Logic 0 Voltage out at 25°C: -1.65 max.
- Operating temperature range: -30 to +85°C
- Storage temperature: -55 to +125°C

*Delays increase or decrease less than 1% for a respective increase or decrease of 5% in supply voltage.

PART NUMBER TABLE

φ DELAYS AND TOLERANCES (in ns)					
Part Number	Rise Time Max.	Output	Part Number	Rise Time Max.	Output
MECLDL-5	3	5 ±1	MECLDL-23	6	23 ±1
MECLDL-6	3	6 ±1	MECLDL-24	6	24 ±1
MECLDL-7	3	7 ±1	MECLDL-25	6	25 ±1
MECLDL-8	3	8 ±1	MECLDL-30	7	30 ±1.5
MECLDL-9	3	9 ±1	MECLDL-35	7	35 ±1.5
MECLDL-10	4	10 ±1	MECLDL-40	8	40 ±1.5
MECLDL-11	4	11 ±1	MECLDL-45	8	45 ±2
MECLDL-12	4	12 ±1	MECLDL-50	9	50 ±2
MECLDL-13	4	13 ±1	MECLDL-55	9	55 ±2
MECLDL-14	4	14 ±1	MECLDL-60	10	60 ±2
MECLDL-15	5	15 ±1	MECLDL-65	10	65 ±2.5
MECLDL-16	5	16 ±1	MECLDL-70	11	70 ±2.5
MECLDL-17	5	17 ±1	MECLDL-75	11	75 ±2.5
MECLDL-18	5	18 ±1	MECLDL-80	12	80 ±2.5
MECLDL-19	5	19 ±1	MECLDL-85	13	85 ±3
MECLDL-20	5	20 ±1	MECLDL-90	13	90 ±3
MECLDL-21	6	21 ±1	MECLDL-95	14	95 ±3
MECLDL-22	6	22 ±1	MECLDL-100	15	100 ±3

φ All modules can be operated with a minimum input pulse width of 100% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. **Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.**