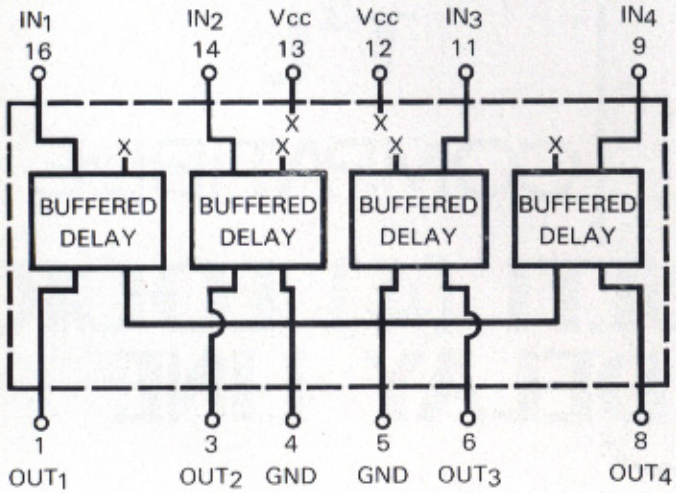
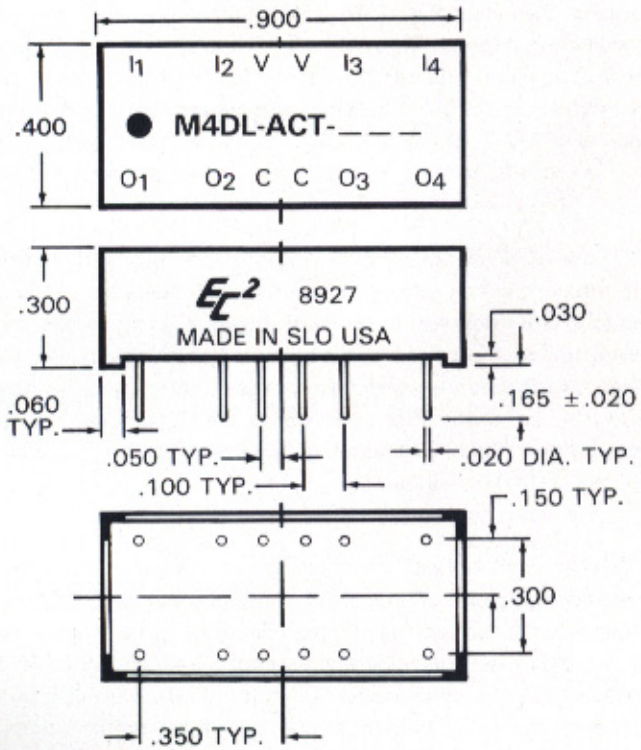
DESIGN NOTES (continued)

Marking consists of manufacturer's name, logo (EC^2), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



OPERATING SPECIFICATIONS

*V_{CC} supply voltage: . . . . . 4.75 to 5.25V DC

V_{CC} supply current:

Constant "1" or "0" in . . . . . 1ma typical

Constant 1 Mhz square wave . . . 25ma typical

Logic 1 input:

Voltage . . . . . 2V min.; V_{CC} max.

Logic 0 input:

Voltage . . . . . 0.8V max.

Logic 1 Voltage out: . . . . . 4.3V min. @ −24ma

Logic 0 Voltage out: . . . . . 0.44V max. @ +24m

Operating temperature range: . . . . . −40 to +85°C.

Storage temperature: . . . . . −55 to +125°C.

*Delays increase or decrease approximately 4% for an increase o decrease of 5% in supply voltage.

PART NUMBER TABLE

ø DELAYS AND TOLERANCES (in ns)			
PART NO.	OUTPUT	PART NO.	OUTPUT
M4DL-ACT-6	6 ±1	M4DL-ACT-30	30 ±1.5
M4DL-ACT-7	7 ±1	M4DL-ACT-35	35 ±1.5
M4DL-ACT-8	8 ±1	M4DL-ACT-40	40 ±1.5
M4DL-ACT-9	9 ±1	M4DL-ACT-45	45 ±2.0
M4DL-ACT-10	10 ±1	M4DL-ACT-50	50 ±2.0
M4DL-ACT-11	11 ±1	M4DL-ACT-55	55 ±2.0
M4DL-ACT-12	12 ±1	M4DL-ACT-60	60 ±2.0
M4DL-ACT-13	13 ±1	M4DL-ACT-65	65 ±2.5
M4DL-ACT-14	14 ±1	M4DL-ACT-70	70 ±2.5
M4DL-ACT-15	15 ±1	M4DL-ACT-75	75 ±2.5
M4DL-ACT-16	16 ±1	M4DL-ACT-80	80 ±2.5
M4DL-ACT-17	17 ±1	M4DL-ACT-85	85 ±3.0
M4DL-ACT-18	18 ±1	M4DL-ACT-90	90 ±3.0
M4DL-ACT-19	19 ±1	M4DL-ACT-95	95 ±3.0
M4DL-ACT-20	20 ±1	M4DL-ACT-100	100 ±3.0
M4DL-ACT-21	21 ±1	M4DL-ACT-125	125 ±4.0
M4DL-ACT-22	22 ±1	M4DL-ACT-150	150 ±4.5
M4DL-ACT-23	23 ±1	M4DL-ACT-175	175 ±5.0
M4DL-ACT-24	24 ±1	M4DL-ACT-200	200 ±6.0
M4DL-ACT-25	25 ±1		

TEST CONDITIONS

1. All measurements are made at 25°C.
2. V_{CC} supply voltage is maintained at 5.0V DC.
3. All units are tested using an ACT toggle-type positive input pulse and one ACT load at the output.
4. ø Input pulse width used is 600ns. Pulse period is 5,000ns.

ø All modules can be operated with a minimum input pulse width of 100% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.