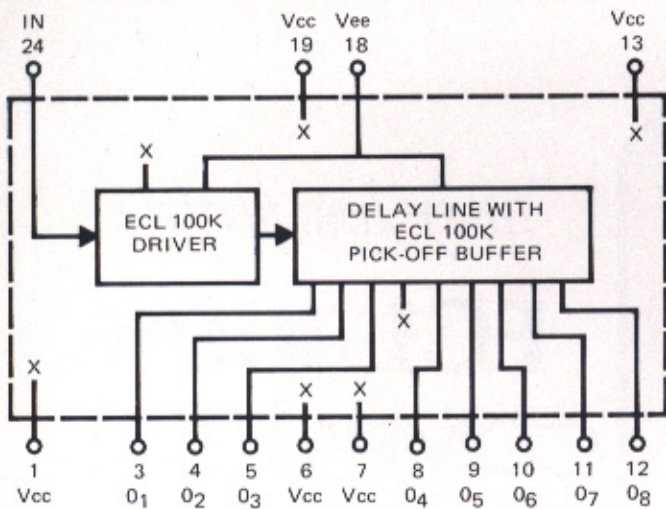
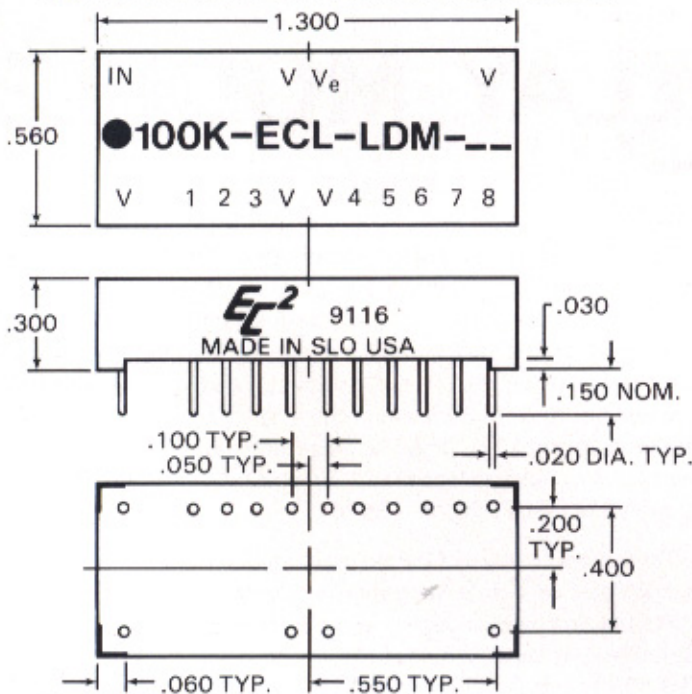


**BLOCK DIAGRAM IS SHOWN BELOW**



**MECHANICAL DETAIL IS SHOWN BELOW**



**TEST CONDITIONS**

1. All measurements are made at 25°C.
2. Vee supply voltage is maintained at -4.5V DC.
3. All units are tested using a positive input pulse provided by a standard open emitter ECL 100K gate. The input and output utilize a 50 ohm pulldown resistor to -2V; the output being tested is also loaded with one ECL 100K gate.
4. Input pulse width used is 5 to 10ns longer than full delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

**OPERATING SPECIFICATIONS**

\*Supply Voltage: . . . . . -4.5V ± 5% to Vee  
 Supply Current: . . . . . 80ma typical

**Logic 1 Input at 25°C:**

Voltage . . . . . -1.165V min.  
 Current . . . . . 350ua max.

**Logic 0 Input at 25°C:**

Voltage . . . . . -1.475V max.  
 Current . . . . . .5ua min.

**Logic 1 Output at 25°C:** . . . . . -1.025V min.

**Logic 0 Output at 25°C:** . . . . . -1.620V max.

Operating temperature range: . . . . . 0 to +85°C.

Storage temperature: . . . . . -55 to +125°C.

\*Delays increase or decrease less than .5% for an increase or decrease of 5% in supply voltage.

**PART NUMBER TABLE**

φ RISE TIME, DELAY AND TOLERANCES (in ns)									
Part Number	Rise Time Max.	Tap1	Tap2	Tap3	Tap4	Tap5	Tap6	Tap7	Output
100K-ECL-LDM-9	2.0	2 ±.2	3 ±.3	4 ±.4	5 ±.5	6 ±.6	7 ±.7	8 ±.8	9 ±.9
100K-ECL-LDM-12.5	2.0	2 ±.2	3.5 ±.35	5 ±.5	6.5 ±.65	8 ±.8	9.5 ±.95	11 ±1	12.5 ±1
100K-ECL-LDM-16	2.0	2 ±.2	4 ±.4	6 ±.6	8 ±.8	10 ±1	12 ±1	14 ±1	16 ±1
100K-ECL-LDM-20	2.0	2.5 ±.25	5 ±.5	7.5 ±.75	10 ±1	12.5 ±1	15 ±1	17.5 ±1	20 ±1
100K-ECL-LDM-24	2.0	3 ±.3	6 ±.6	9 ±.9	12 ±1	15 ±1	18 ±1	21 ±1	24 ±1
100K-ECL-LDM-28	2.0	3.5 ±.35	7 ±.7	10.5 ±1	14 ±1	17.5 ±1	21 ±1	24.5 ±1	28 ±1
100K-ECL-LDM-32	2.5	4 ±.4	8 ±.8	12 ±1	16 ±1	20 ±1	24 ±1	28 ±1	32 ±1
100K-ECL-LDM-36	2.5	4.5 ±.45	9 ±.9	13.5 ±1	18 ±1	22.5 ±1	27 ±1	31.5 ±1	36 ±1
100K-ECL-LDM-40	2.5	5 ±.5	10 ±1	15 ±1	20 ±1	25 ±1	30 ±1	35 ±1	40 ±1.5
100K-ECL-LDM-44	3.0	5.5 ±.55	11 ±1	16.5 ±1	22 ±1	27.5 ±1	33 ±1	38.5 ±1	44 ±1.5
100K-ECL-LDM-48	3.0	6 ±.6	12 ±1	18 ±1	24 ±1	30 ±1	36 ±1	42 ±1.5	48 ±2
100K-ECL-LDM-52	3.0	6.5 ±.65	13 ±1	19.5 ±1	26 ±1	32.5 ±1	39 ±1.5	45.5 ±2	52 ±2
100K-ECL-LDM-56	3.0	7 ±.7	14 ±1	21 ±1	28 ±1	35 ±1	42 ±1.5	49 ±2	56 ±2
100K-ECL-LDM-60	4.0	7.5 ±.75	15 ±1	22.5 ±1	30 ±1	37.5 ±1	45 ±1.5	52.5 ±2	60 ±2
100K-ECL-LDM-64	4.0	8 ±.8	16 ±1	24 ±1	32 ±1	40 ±1.5	48 ±2	56 ±2	64 ±2
100K-ECL-LDM-68	4.0	8.5 ±.85	17 ±1	25.5 ±1	34 ±1	42.5 ±1.5	51 ±2	59.5 ±2	68 ±2
100K-ECL-LDM-72	4.5	9 ±.9	18 ±1	27 ±1	36 ±1	45 ±1.5	54 ±2	63 ±2	72 ±2.5
100K-ECL-LDM-76	4.5	9.5 ±.95	19 ±1	28.5 ±1	38 ±1	47.5 ±2	57 ±2	66.5 ±2	76 ±2.5
100K-ECL-LDM-80	4.5	10 ±1	20 ±1	30 ±1	40 ±1.5	50 ±2	60 ±2	70 ±2	80 ±2.5

φ All modules can be operated with a minimum input pulse width of 25% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. **Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.**