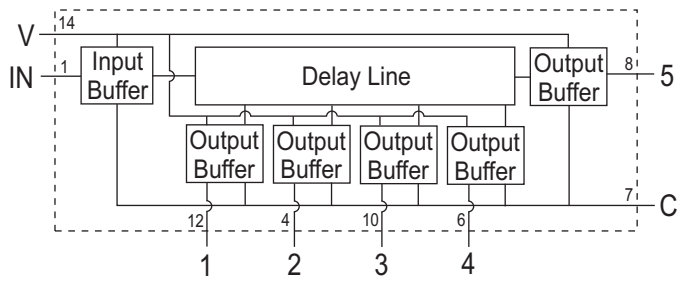
CMOS Logic Delay Module (Thin Profile Package)

The CMOS Logic Delay Modules (Thin Profile Package) manufactured by Engineered Components Company are designed to provide output waveforms that reproduce the input waveform after a set amount of delay time has elapsed. The five output waveforms are delay line taps provided at 20% increments of the total delay (20, 40, 60, 80, and 100%). These delay modules are non-inverting. The delay times are calibrated to the listed tolerances on the rising edge delays. The products with a total delay of less than 75ns have additional delay present at tap 1 due to internal propagation delays (see the Product Selection Table).

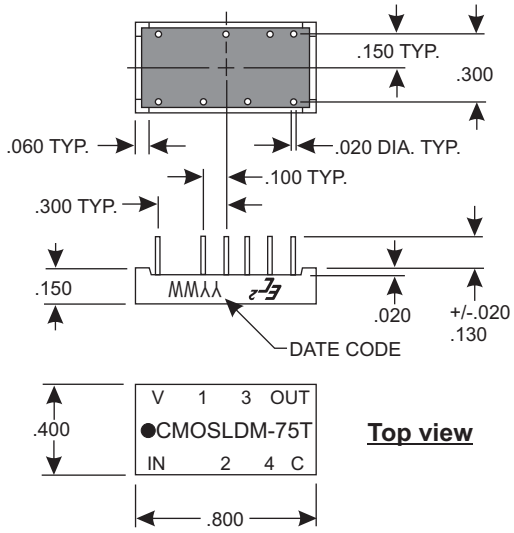
The MTBF on these modules, when calculated per MIL-HDBK-217, for a 50 deg.C ground fixed environment and with 50VDC applied, is in excess of 3 million hours. The temperature coefficient of delay is less than 270 ppm/deg.C or 3ns, whichever is greater, over the operating temperature range of -40 to +85 deg. C.

The module is provided in a 14-pin DIP package, fully encapsulated in epoxy resin and is housed in a Diallyl Phthalate case, blue in color. The case marking is applied by silkscreen using white epoxy paint. The 8 copper leads are tin-lead plated and meet the solderability requirements of MIL-STD-202, Method 208.

BLOCK DIAGRAM



MECHANICAL DIAGRAM



Top view

Product Selection Table

Part Number	Output Delay and Tolerances (in ns)				
	Tap 1 (20%)	Tap 2 (40%)	Tap 3 (60%)	Tap 4 (80%)	Tap 5 (100%)
CMOSLDM-26T	16.0+/-1.0	18.5+/-1.0	21.0+/-1.0	23.5+/-1.0	26.0+/-1.0
CMOSLDM-28T	16.0+/-1.0	19.0+/-1.0	22.0+/-1.0	25.0+/-1.0	28.0+/-1.0
CMOSLDM-32T	16.0+/-1.0	20.0+/-1.0	24.0+/-1.0	28.0+/-1.0	32.0+/-1.0
CMOSLDM-35T	15.0+/-1.0	20.0+/-1.0	25.0+/-1.0	30.0+/-1.5	35.0+/-1.5
CMOSLDM-39T	15.0+/-1.0	21.0+/-1.0	27.0+/-1.5	33.0+/-1.5	39.0+/-1.5
CMOSLDM-43T	15.0+/-1.0	22.0+/-1.0	29.0+/-1.5	36.0+/-1.5	43.0+/-1.5
CMOSLDM-47T	15.0+/-1.0	23.0+/-1.0	31.0+/-1.5	39.0+/-1.5	47.0+/-1.5
CMOSLDM-51T	15.0+/-1.0	24.0+/-1.0	33.0+/-1.5	42.0+/-1.5	51.0+/-2.0
CMOSLDM-55T	15.0+/-1.0	25.0+/-1.0	35.0+/-1.5	45.0+/-2.0	55.0+/-2.0
CMOSLDM-59T	15.0+/-1.0	26.0+/-1.0	37.0+/-1.5	48.0+/-2.0	59.0+/-2.5
CMOSLDM-63T	15.0+/-1.0	27.0+/-1.0	39.0+/-1.5	51.0+/-2.0	63.0+/-2.5
CMOSLDM-67T	15.0+/-1.0	28.0+/-1.5	41.0+/-1.5	54.0+/-2.0	67.0+/-2.5
CMOSLDM-71T	15.0+/-1.0	29.0+/-1.5	43.0+/-1.5	57.0+/-2.0	71.0+/-2.5
CMOSLDM-75T	15.0+/-1.0	30.0+/-1.5	45.0+/-2.0	60.0+/-2.5	75.0+/-2.5
CMOSLDM-80T	16.0+/-1.0	32.0+/-1.5	48.0+/-2.0	64.0+/-2.5	80.0+/-3.0
CMOSLDM-85T	17.0+/-1.0	34.0+/-1.5	51.0+/-2.0	68.0+/-2.5	85.0+/-3.0
CMOSLDM-90T	18.0+/-1.0	36.0+/-1.5	54.0+/-2.0	72.0+/-2.5	90.0+/-3.0
CMOSLDM-95T	19.0+/-1.0	38.0+/-1.5	57.0+/-2.0	76.0+/-2.5	95.0+/-3.0
CMOSLDM-100T	20.0+/-1.0	40.0+/-1.5	60.0+/-2.0	80.0+/-3.0	100.0+/-3.0
CMOSLDM-125T	25.0+/-1.0	50.0+/-2.0	75.0+/-2.5	100.0+/-3.0	125.0+/-4.0
CMOSLDM-150T	30.0+/-1.5	60.0+/-2.0	90.0+/-3.0	120.0+/-4.0	150.0+/-5.0
CMOSLDM-175T	35.0+/-1.5	70.0+/-2.5	105.0+/-4.0	140.0+/-5.0	175.0+/-5.0
CMOSLDM-200T	40.0+/-1.5	80.0+/-3.0	120.0+/-4.0	160.0+/-5.0	200.0+/-6.0
CMOSLDM-225T	45.0+/-2.0	90.0+/-3.0	135.0+/-4.0	180.0+/-6.0	225.0+/-7.0
CMOSLDM-250T	50.0+/-2.0	100.0+/-3.0	150.0+/-5.0	200.0+/-6.0	250.0+/-8.0

Special modules can often be manufactured to provide for customer specific applications.

Operating Specifications:

All measurements made at 25 deg. C
All measurements made with Vcc = +5VDC
All measurements made with (1) CMOS output load

Operating Temperature: -40 to +85 deg. C
Storage Temperature: -55 to +125 deg. C

Vcc Supply Voltage: 4.5 to 5.5VDC
Vcc Supply Current:
  Constant “0” in = 7 to 13mA typical
  Constant “1” in = 0.1uA typical
Logic “High” Input:
  Voltage: 2.0VDC min. ; Vcc max.
  Current: 2.4VDC = 1.0uA max.
Logic “Low” Input:
  Voltage: 0.8 VDC max.
  Current: 1.0uA max.
Logic “High” Voltage Out: 3.84VDC min.
Logic “Low” Voltage Out: 0.33VDC max.

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